

Features

- 13–25 GHz Low-Noise and Driver Amplifier
- 16 dBm Typical Output P1dB
- 23 dB Small-Signal Gain
- 1.9 dB Typical Noise Figure
- > 8 dB Return Loss Input and Output
- +4 V, 65 mA Nominal Bias
- 16 Lead QFN, 2.5 mm × 2.5 mm

Applications

- ISM
- VSAT
- Point-to-Point Radios

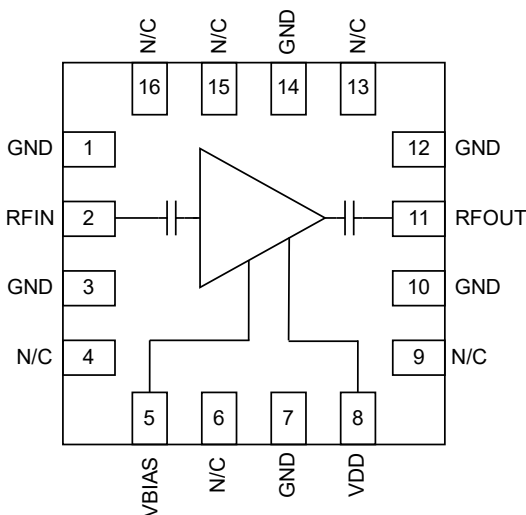
Description

ARF1205Q2 is a low-noise and driver amplifier designed for high data-rate applications. With 23 dB of linear gain, 1.9 dB noise figure, 17 dBm output P1dB and low-current operation, it is well suited to demanding, high-order modulation schemes. The circuit typically draws 65 mA from a 4 V DC supply in buffer amplifier bias, or 40 mA from a 3.3 V supply in low-noise bias. The part is internally matched to 50 Ω with ESD protection. The part has internal bias regulation controlled by V_{BIAS} , or alternatively by a resistor between V_{DD} and V_{BIAS} .

The part is RoHS* compliant and built with the latest manufacturing techniques to optimize for reliability and quality.

Export from The Netherlands/EU, no licence.

Functional Diagram



All not connected (N/C) pins should be connected to RF and thermal ground.

Pin	Pin Name	Description
2	RF _{IN}	RF Input
5	V _{BIAS}	Current Control & Power Down
8	V _{DD}	Power Supply
11	RF _{OUT}	RF Output
1, 3, 7, 10, 12, 14, Paddle	GND	Ground
4, 6, 9, 13, 15, 16	N/C	Unconnected Pins.

*RoHS compliant – European Union Directive 2011/65/EU

Electrical Specifications, Buffer Amplifier Bias^{1,2}

Parameter	Test Conditions	Min	Typ	Max	Units
Frequency Range		13		25	GHz
Small Signal Gain	13 GHz 16 GHz 22 GHz 25 GHz	24.5 25.5 20.0 19.5	26.5 27.5 22.0 21.5	28.5 29.5 24.0 23.5	dB
Gain Variation over Temperature			0.01		dB/°C
Noise Figure	13 GHz 16 GHz 22 GHz 25 GHz		2.4 2.0 2.0 2.0		dB
Input Return Loss	13 GHz 16 GHz 22 GHz 25 GHz		8 14 19 7		dB
Output Return Loss	13 GHz 16 GHz 22 GHz 25 GHz		14 11 8 8		dB
Reverse Isolation	13 GHz 16 GHz 22 GHz 25 GHz		56 50 47 48		dB
Output P1dB	13 GHz 16 GHz 22 GHz 25 GHz		14.5 16.0 17.4 15.5		dBm
Output IP3	13 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz 16 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz 22 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz 25 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz		24.0 26.5 27.0 27.5		dBm
V _{DD} Voltage	Safe Operating Range: 0 to 4.0 V	3.0	4.0	4.0	V
I _{DD} Current	V _{BIAS} = 3.3 V, V _{DD} = 4.0 V	58	65	70	mA
	V _{BIAS} = 4.0 V, V _{DD} = 4.0 V			90	mA
V _{BIAS} Voltage	Nominal Bias		3.3		V
	Operating Range	0		4.0	V
I _{BIAS} Current	V _{BIAS} = 3.3 V, V _{DD} = 4.0 V		1.1		mA

- Parameters tested at 25°C in laboratory environment with standard 50 Ω matched equipment.
- Nominal bias of V_{DD} = 4.0 V and V_{BIAS} = 3.3 V (I_{DD} ≈ 65 mA).

Electrical Specifications, Low-Noise Amplifier Bias^{1,2}

Parameter	Test Conditions	Min	Typ	Max	Units
Frequency Range		13		25	GHz
Small Signal Gain	13 GHz 16 GHz 22 GHz 25 GHz		25 26 21 20		dB
Gain Variation over Temperature			0.01		dB/°C
Noise Figure	13 GHz 16 GHz 22 GHz 25 GHz		2.4 1.9 1.9 1.7		dB
Input Return Loss	13 GHz 16 GHz 22 GHz 25 GHz		7 13 18 7		dB
Output Return Loss	13 GHz 16 GHz 22 GHz 25 GHz		14 11 8 8		dB
Reverse Isolation	13 GHz 16 GHz 22 GHz 25 GHz		60 50 48 48		dB
Output P1dB	13 GHz 16 GHz 22 GHz 25 GHz		10.5 12.0 14.5 14.0		dBm
Output IP3	13 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz 16 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz 22 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz 25 GHz, P _{OUT} /tone = +5 dBm, ΔF = 10 MHz		18.5 22.0 23.5 25.0		dBm
V _{DD} Voltage	Safe Operating Range: 0 to 4.0 V	3.0	3.3	4.0	V
I _{DD} Current	V _{BIAS} = 2.5 V, V _{DD} = 3.3 V		40		mA
	V _{BIAS} = 4.0 V, V _{DD} = 4.0 V			90	mA
V _{BIAS} Voltage	Nominal Bias		2.5		V
	Operating Range	0		4.0	V
I _{BIAS} Current	V _{BIAS} = 2.5 V, V _{DD} = 3.3 V		0.9		mA

3. Nominal bias of V_{DD} = 3.3 V and V_{BIAS} = 2.5 V (I_{DD} ≈ 40 mA).

Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Units
V_{DD} Voltage		0	4.4	V
I_{DD} Current		0	100	mA
V_{BIAS} Voltage		0	4.4	V
Total Dissipated Power			0.8	W
Maximum RF Input Power	Peak Power		+14	dBm
Channel Temperature			+175	°C
Operating Temperature Range		-40	+85	°C
Storage Temperature Range		-50	+125	°C
Moisture Sensitivity Level	IPC/JEDEC J-STD-020E	MSL1		
ESD Human Body Model (HBM)	JEDEC JS-001-2023	Class 1B		
ESD Charged Device Model (CDM)	JEDEC JS-002-2022	Class C3		

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD Sensitive Device

These devices are ESD sensitive. Proper handling for assembly and use must be maintained at all times. Please see JEDEC JESD625B for further information.

Thermal and Reliability Data

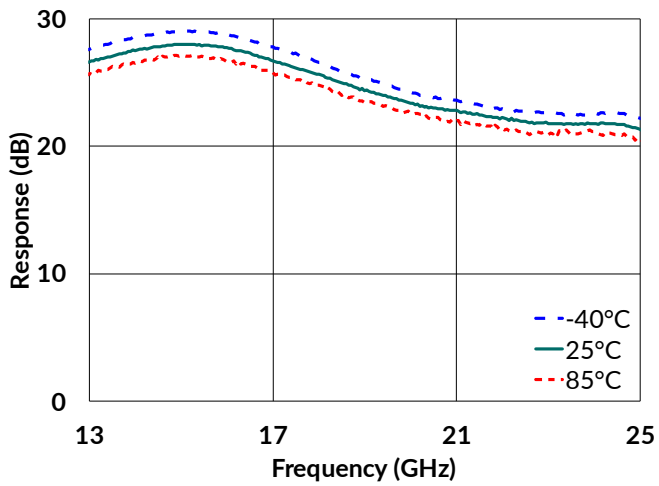
Parameter	Conditions ^{2,4}	Value	Units
Thermal Resistance (R_{TH}) ⁵	$V_{DD} = 4\text{ V}$, $I_{DDQ} = 65\text{ mA}$, Small Signal RF $V_{DD} = 4\text{ V}$, $I_{DDQ} = 65\text{ mA}$, $P_{OUT} = 17.5\text{ dBm}$	194.2 212.5	°C/W
Channel Temperature (T_{CH})	$V_{DD} = 4\text{ V}$, $I_{DDQ} = 65\text{ mA}$, Small Signal RF $V_{DD} = 4\text{ V}$, $I_{DDQ} = 65\text{ mA}$, $P_{OUT} = 17.5\text{ dBm}$	135.5 127.5	°C
Mean Time To Failure (MTTF)	$V_{DD} = 4\text{ V}$, $I_{DDQ} = 65\text{ mA}$, Small Signal RF $V_{DD} = 4\text{ V}$, $I_{DDQ} = 65\text{ mA}$, $P_{OUT} = 17.5\text{ dBm}$	$> 10^7$ $> 10^7$	Hours

- All thermal and reliability data is measured or simulated with 85°C at the package base (solder junction).
- Thermal resistance is the difference between the package base (solder junction) temperature and the channel temperature, divided by the DC power consumption.

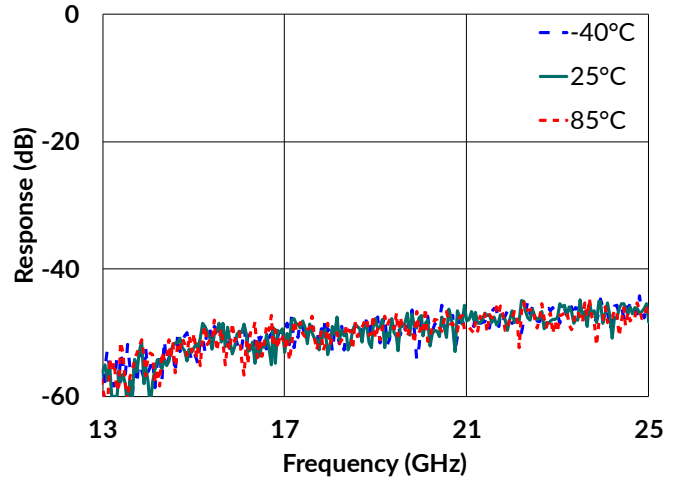
Measured Performance – Small Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 3.3\text{ V}$ ($I_{DD} \approx 65\text{ mA}$)

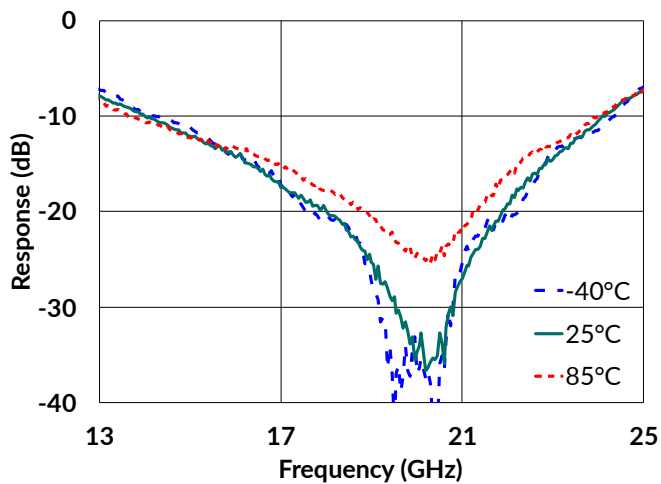
Gain



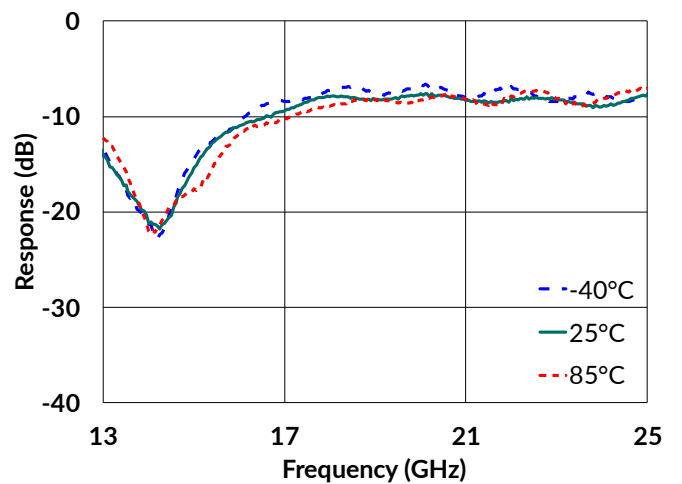
Reverse Isolation



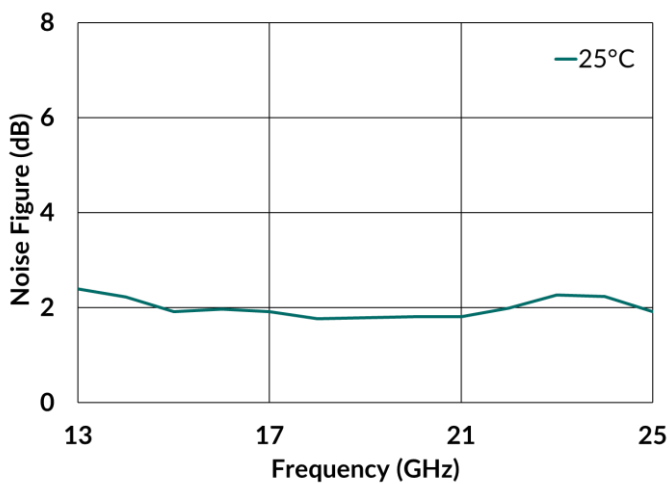
Input Return Loss



Output Return Loss



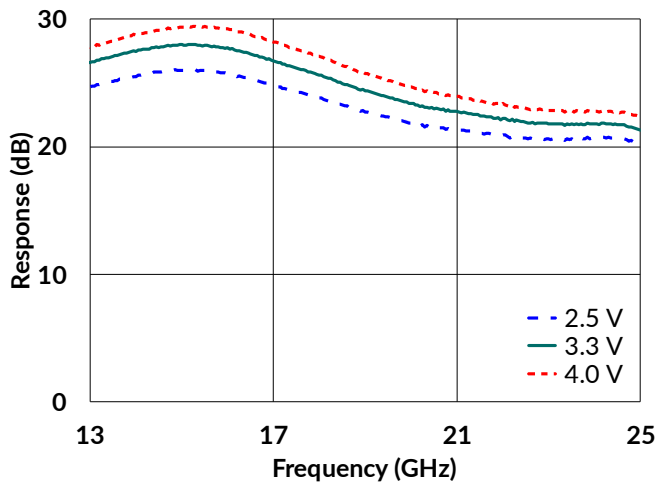
Noise Figure



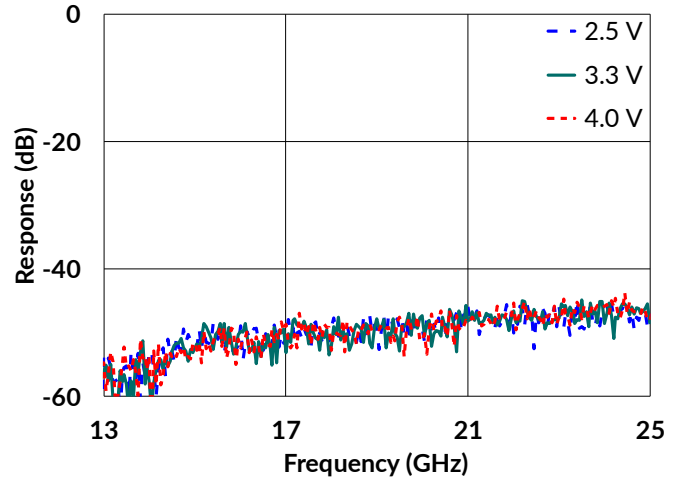
Measured Performance – Small Signal

Room Temperature: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 2.5, 3.3\text{ and }4\text{ V}$ ($I_{DD} \approx 40, 65\text{ and }85\text{ mA}$)

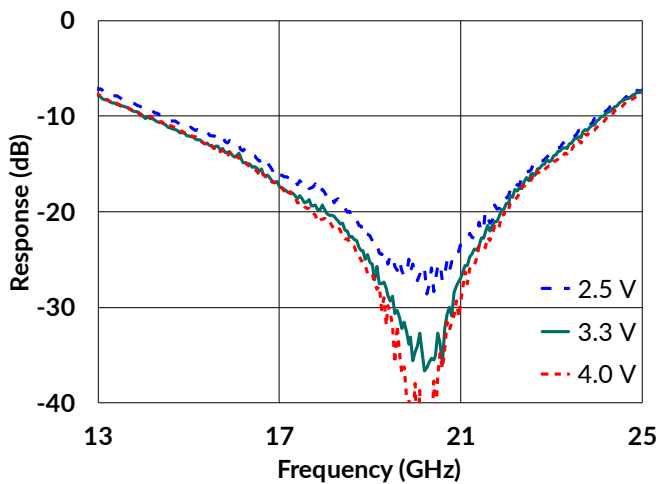
Gain



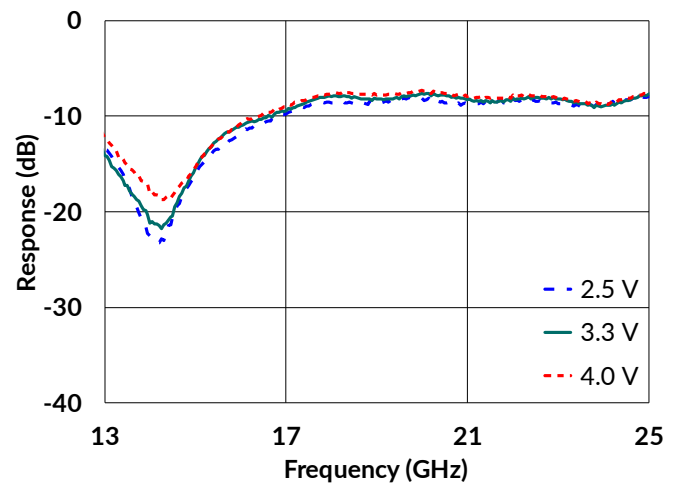
Reverse Isolation



Input Return Loss



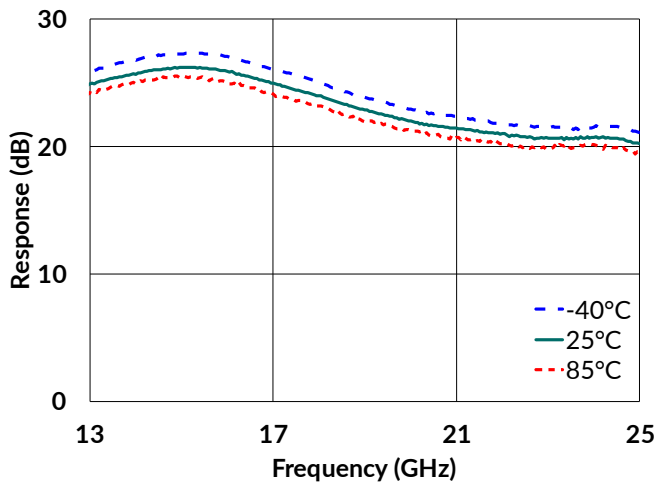
Output Return Loss



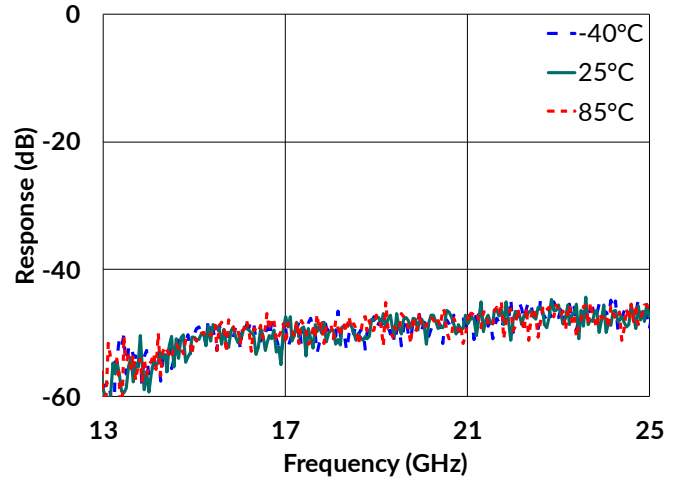
Measured Performance – Small Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 2.5\text{ V}$ ($I_{DD} \approx 40\text{ mA}$)

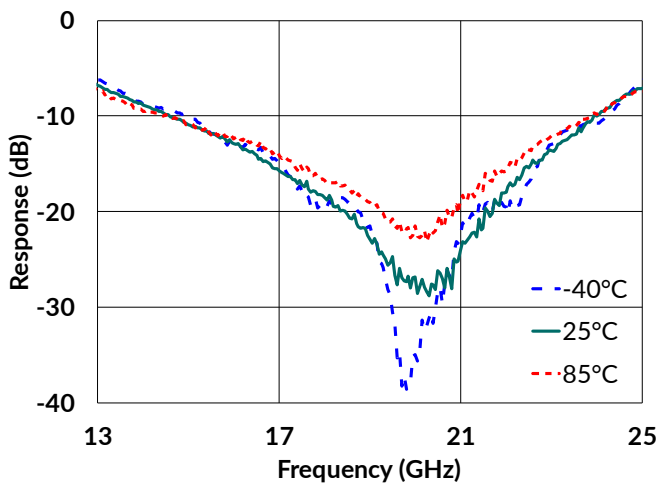
Gain



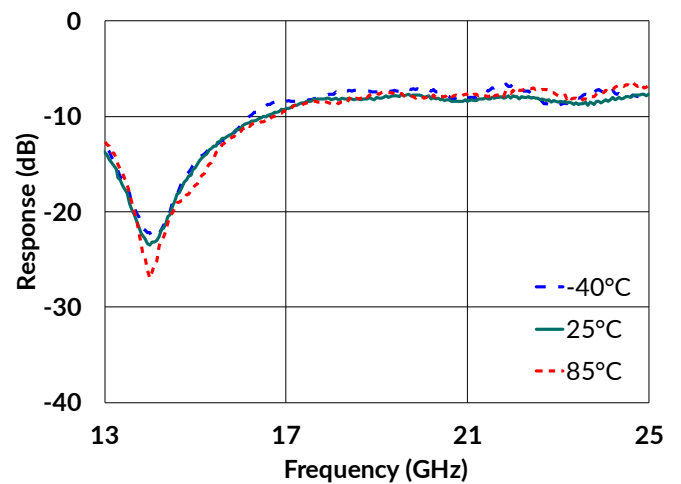
Reverse Isolation



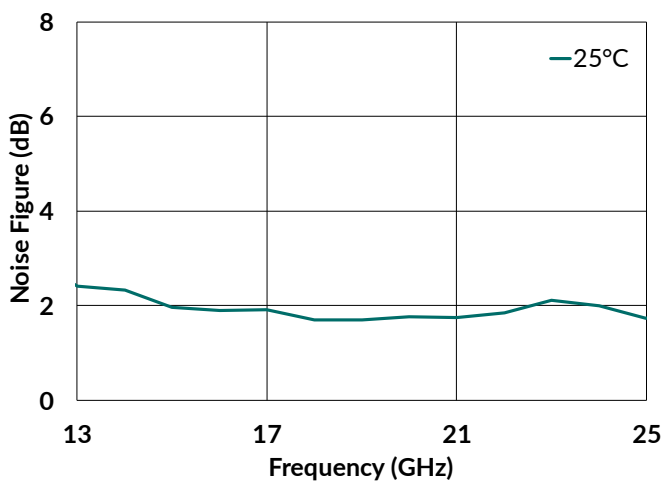
Input Return Loss



Output Return Loss



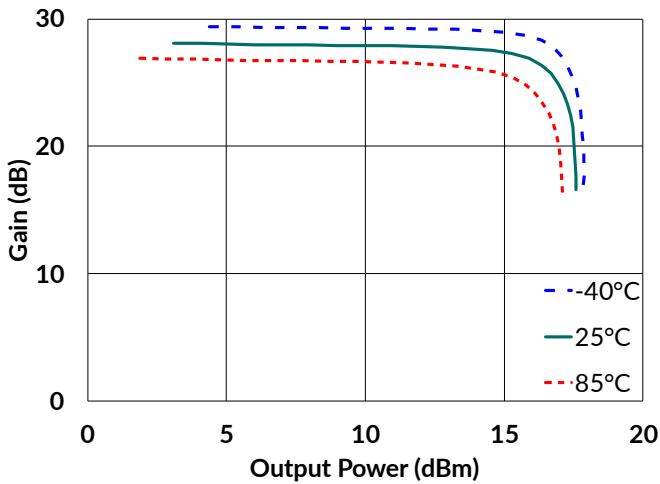
Noise Figure



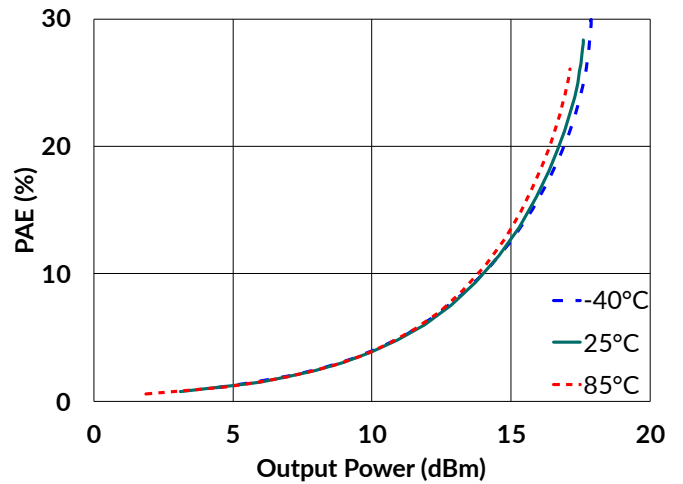
Measured Performance – Large Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 3.3\text{ V}$ ($I_{DDQ} \approx 65\text{ mA}$)

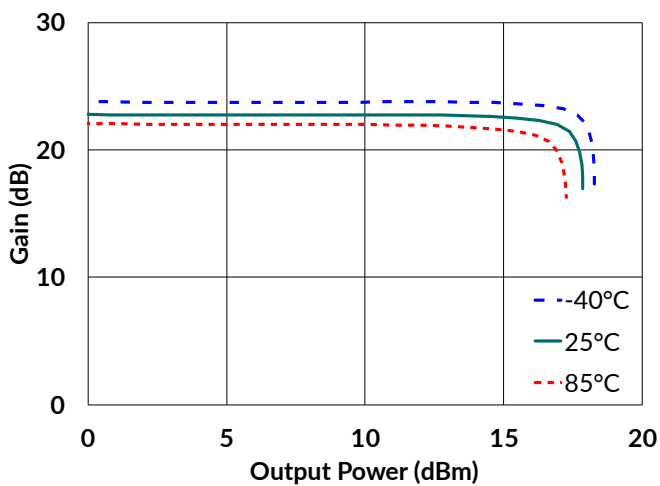
Gain vs Output Power at 16 GHz



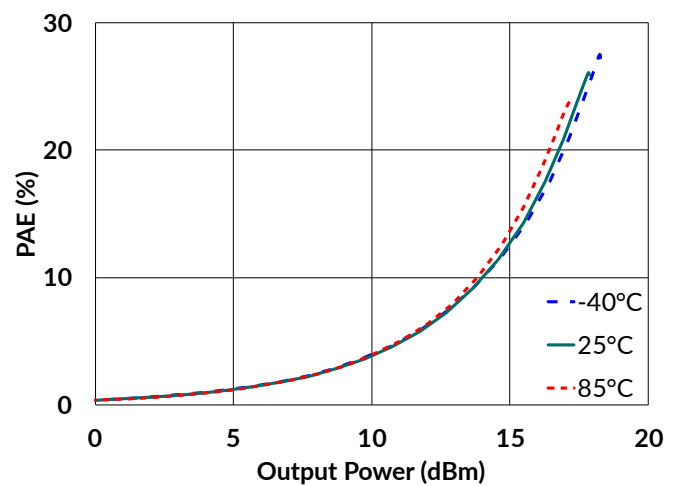
PAE vs Output Power at 16 GHz



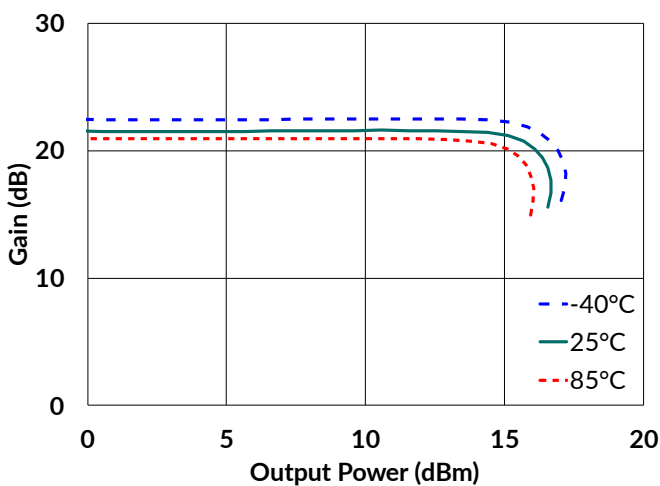
Gain vs Output Power at 22 GHz



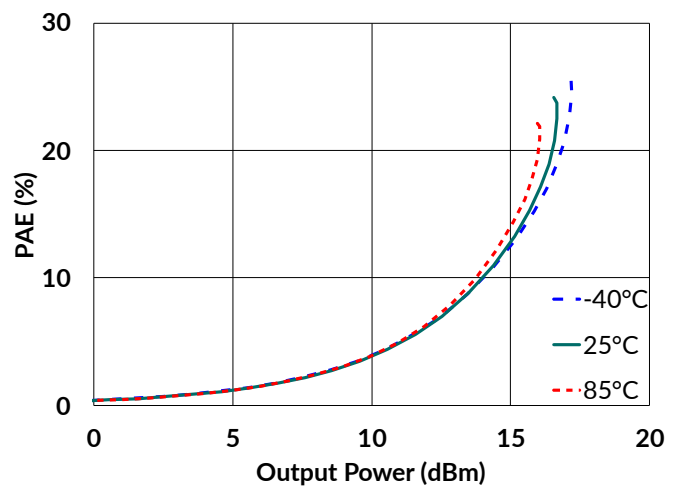
PAE vs Output Power at 22 GHz



Gain vs Output Power at 25 GHz



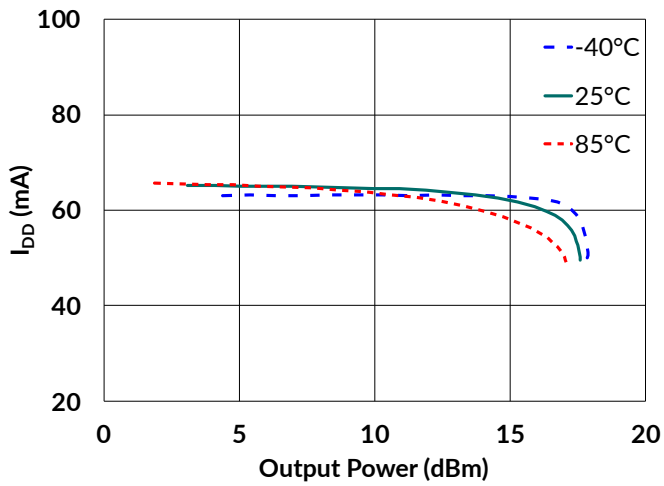
PAE vs Output Power at 25 GHz



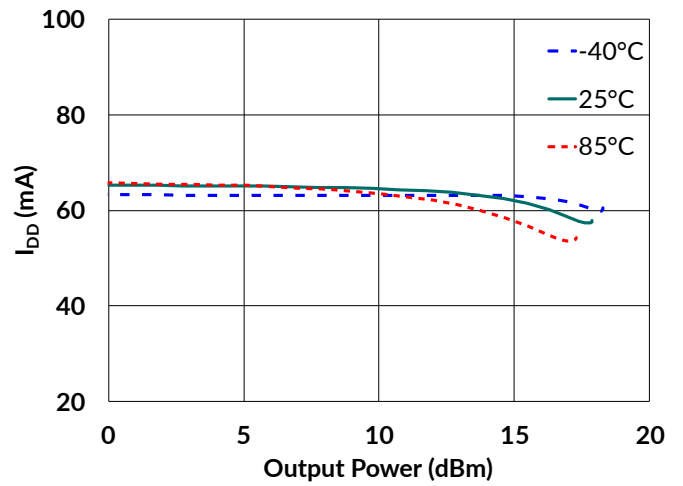
Measured Performance – Large Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 3.3\text{ V}$ ($I_{DDQ} \approx 65\text{ mA}$)

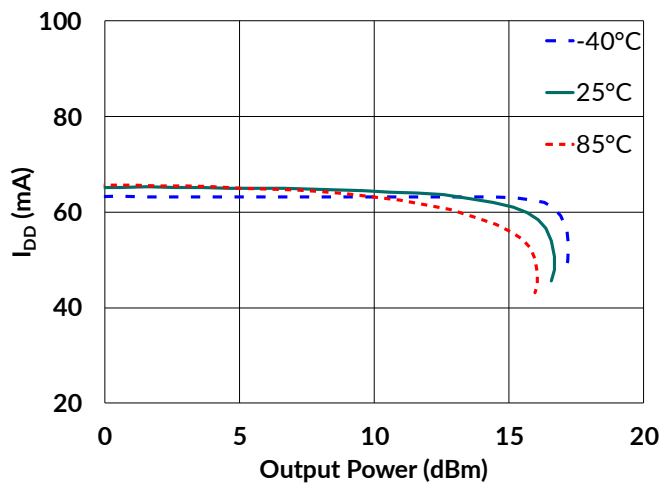
I_{DD} vs Output Power at 16 GHz



I_{DD} vs Output Power at 22 GHz



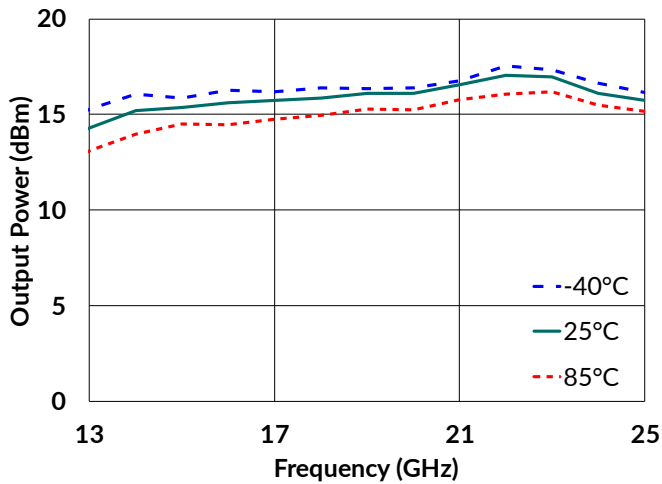
I_{DD} vs Output Power at 25 GHz



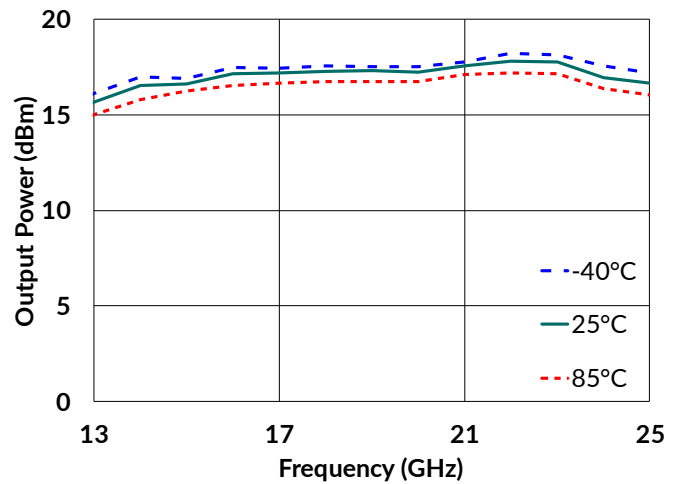
Measured Performance – Large Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 3.3\text{ V}$ ($I_{DDQ} \approx 65\text{ mA}$)

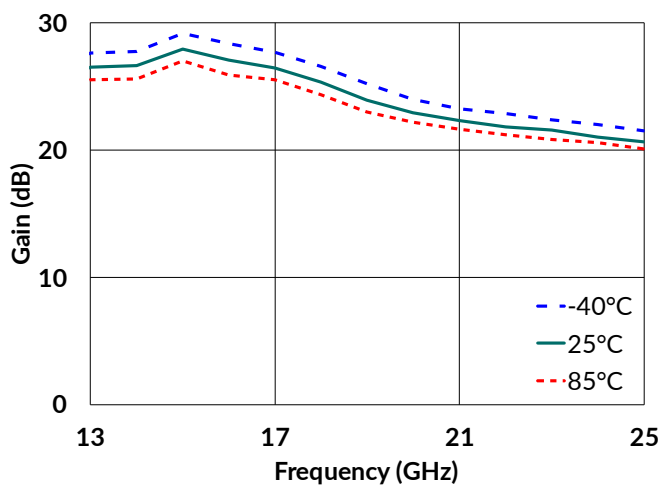
Output P1dB



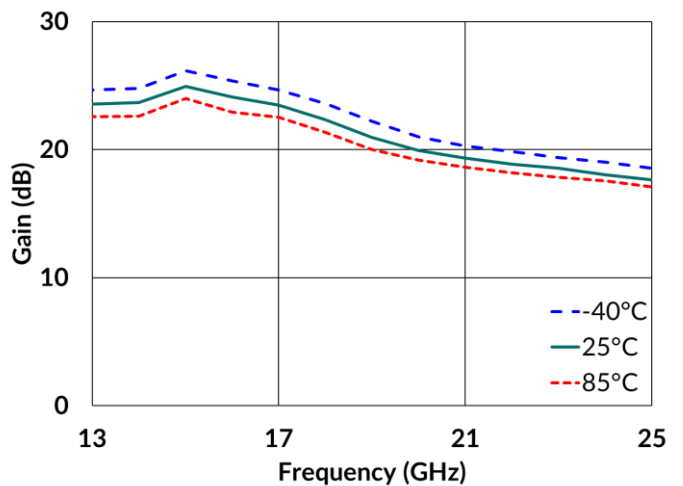
Output P3dB



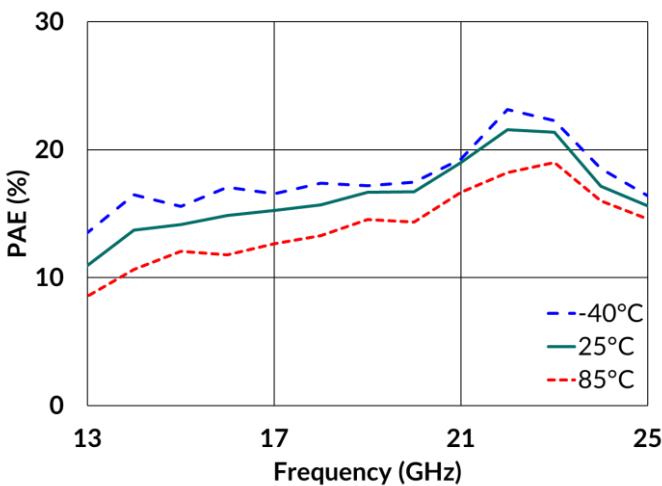
Gain P1dB



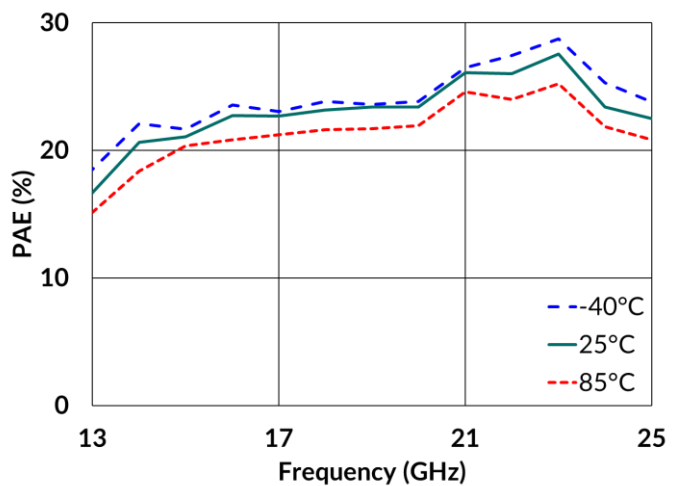
Gain P3dB



PAE P1dB



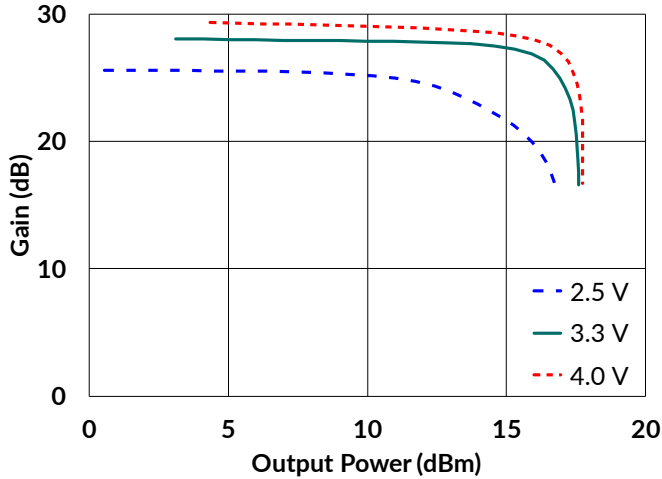
PAE P3dB



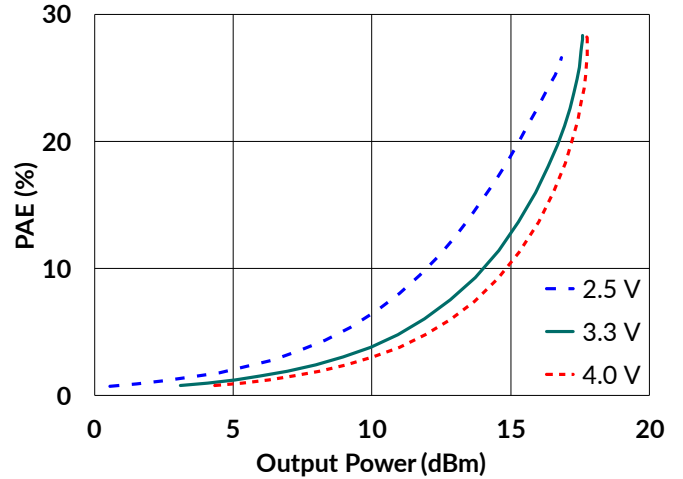
Measured Performance – Large Signal

Room Temperature: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 2.5, 3.3\text{ and }4\text{ V}$ ($I_{DDQ} \approx 40, 65\text{ and }85\text{ mA}$)

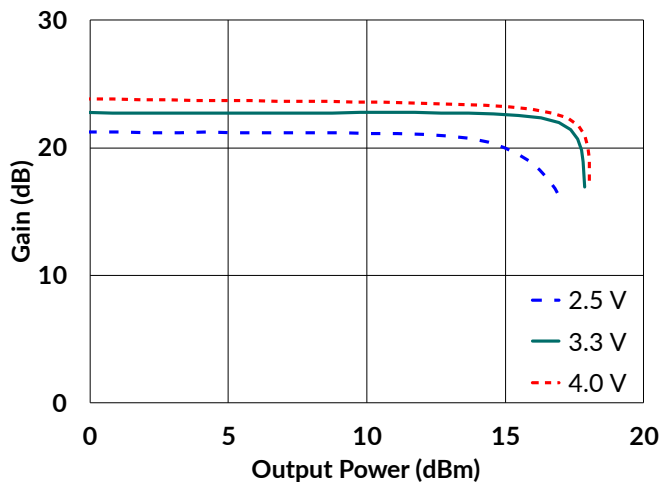
Gain vs Output Power at 16 GHz



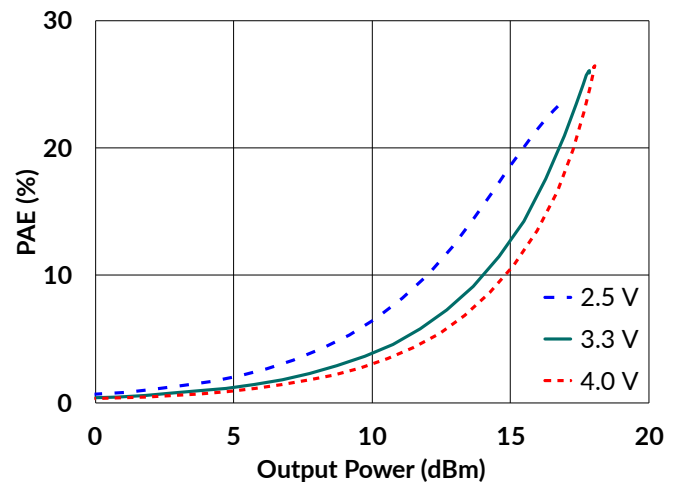
PAE vs Output Power at 16 GHz



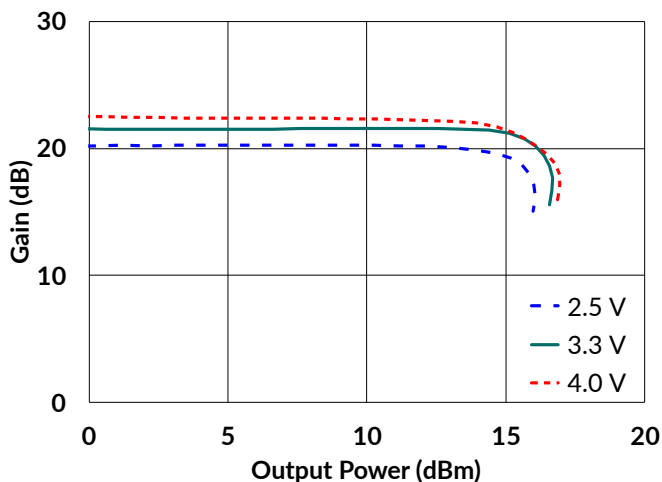
Gain vs Output Power at 22 GHz



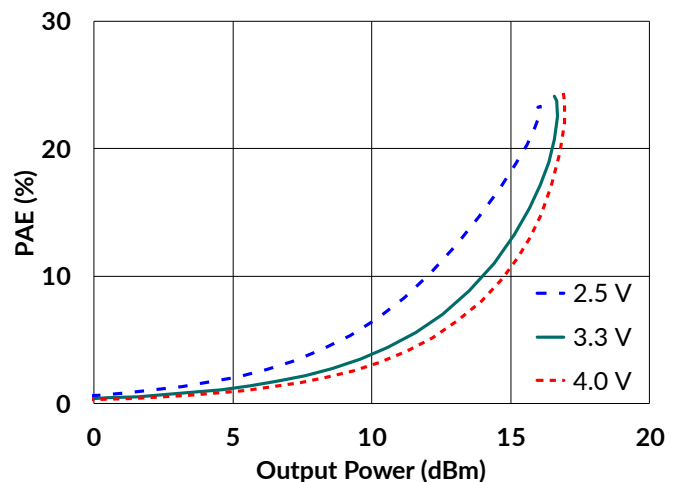
PAE vs Output Power at 22 GHz



Gain vs Output Power at 25 GHz



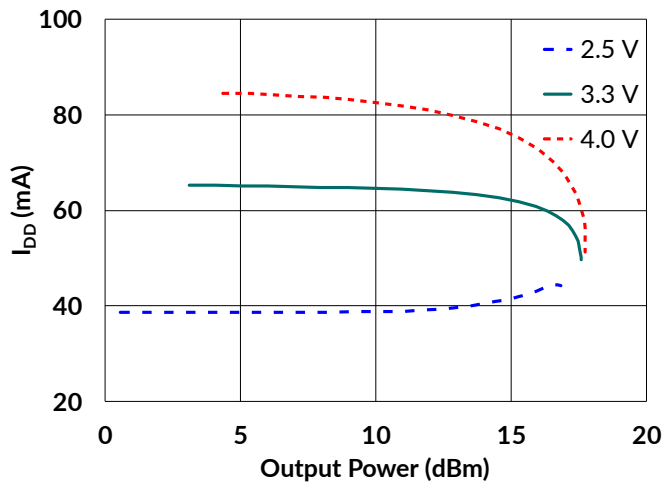
PAE vs Output Power at 25 GHz



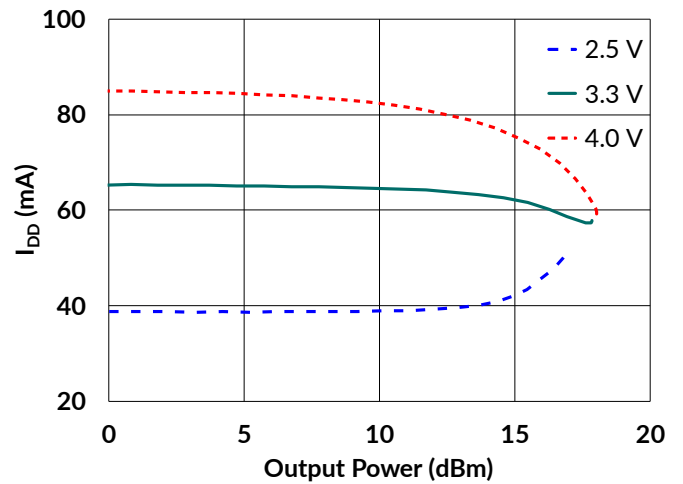
Measured Performance – Large Signal

Room Temperature: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 2.5, 3.3\text{ and }4\text{ V}$ ($I_{DDQ} \approx 40, 65\text{ and }85\text{ mA}$)

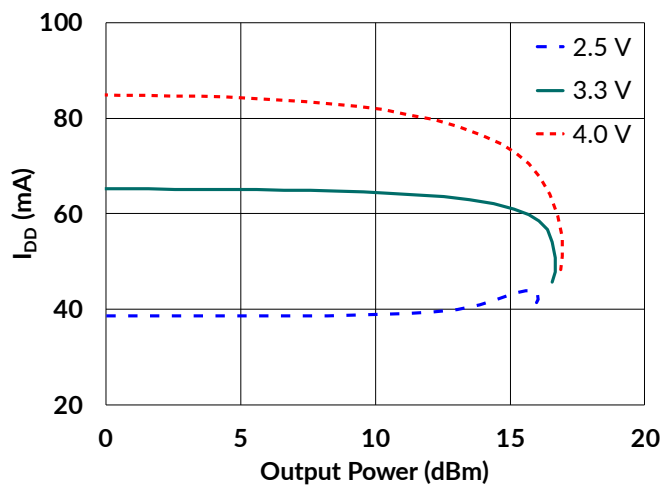
I_{DD} vs Output Power at 16 GHz



I_{DD} vs Output Power at 22 GHz



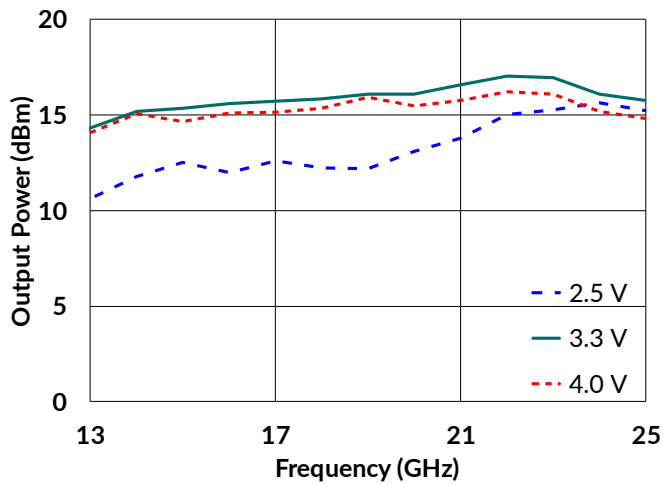
I_{DD} vs Output Power at 25 GHz



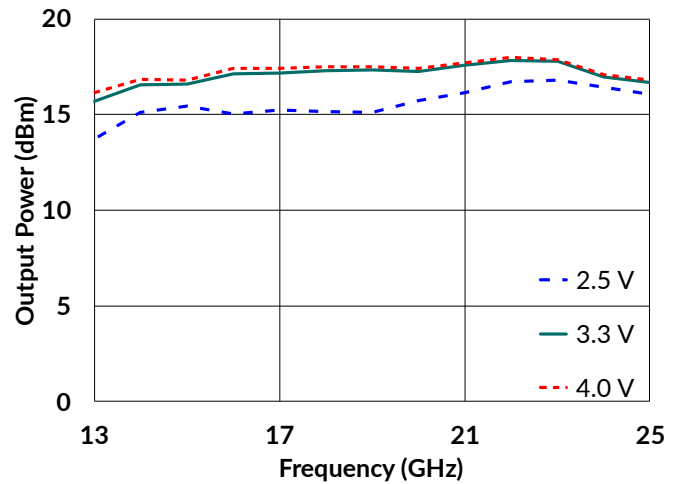
Measured Performance – Large Signal

Room Temperature: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 2.5, 3.3\text{ and }4\text{ V}$ ($I_{DDQ} \approx 40, 65\text{ and }85\text{ mA}$)

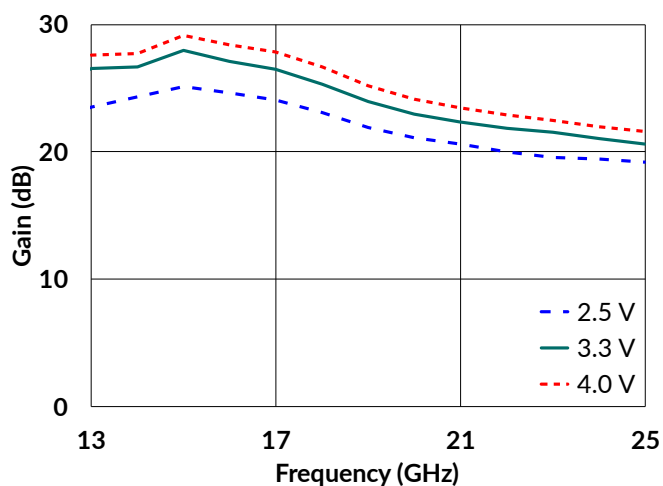
Output P1dB



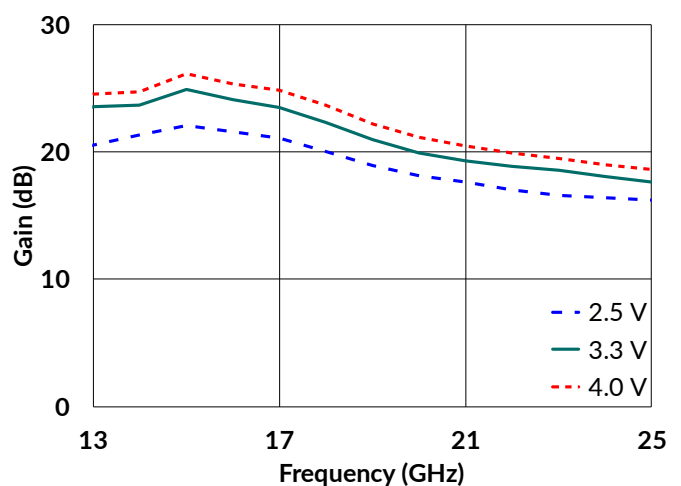
Output P3dB



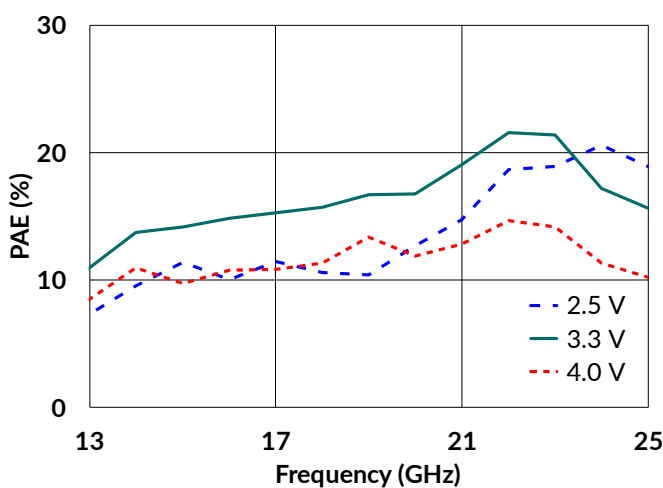
Gain P1dB



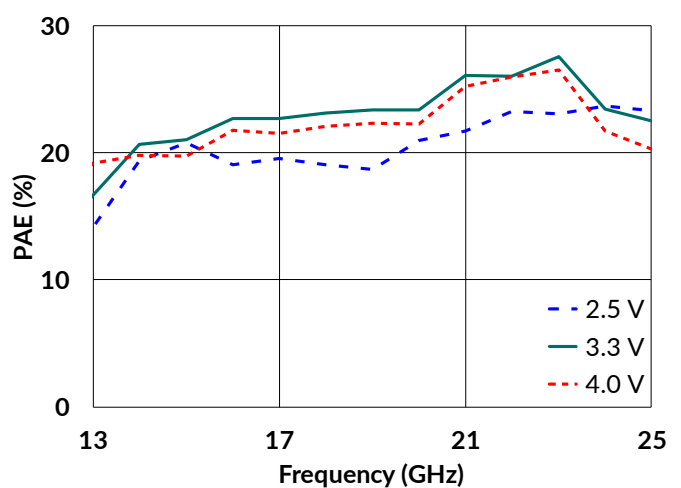
Gain P3dB



PAE P1dB



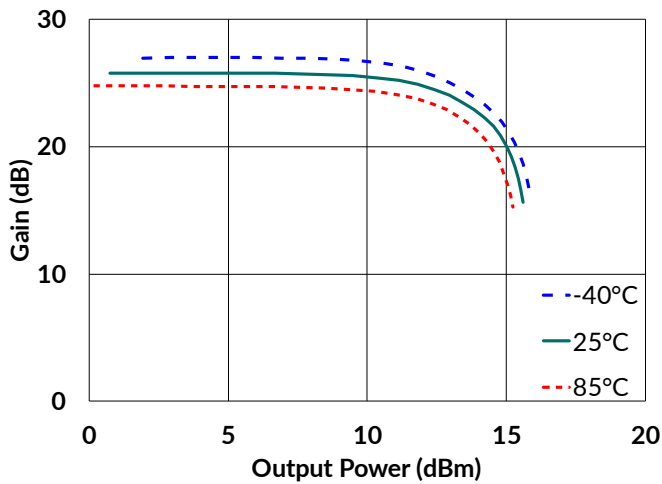
PAE P3dB



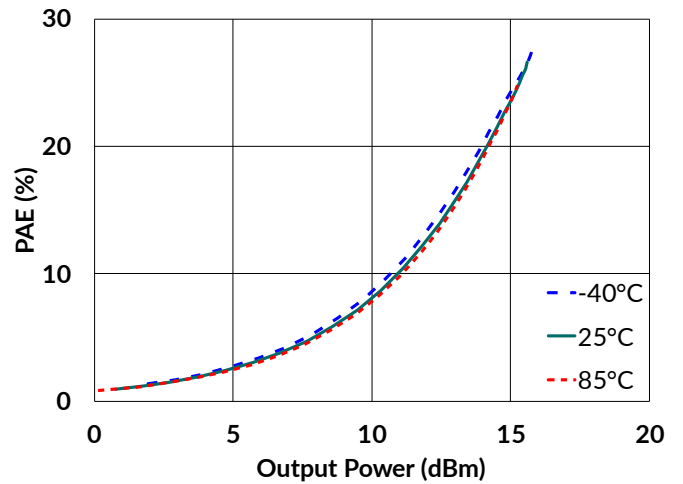
Measured Performance – Large Signal

Nominal Bias: $V_{DD} = 3.3\text{ V}$, $V_{BIAS} = 2.5\text{ V}$ ($I_{DDQ} \approx 40\text{ mA}$)

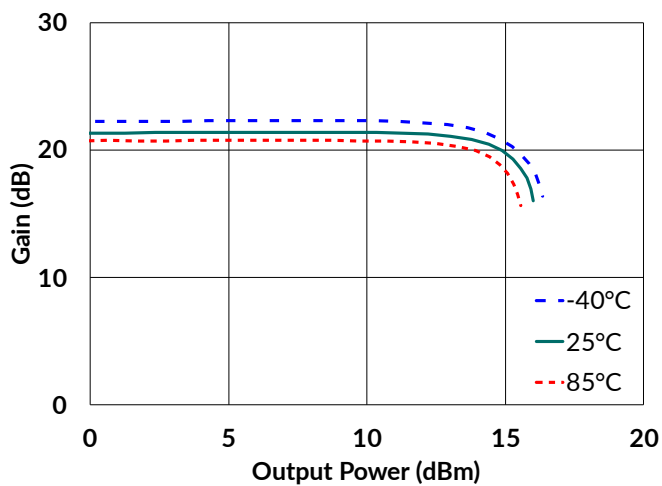
Gain vs Output Power at 16 GHz



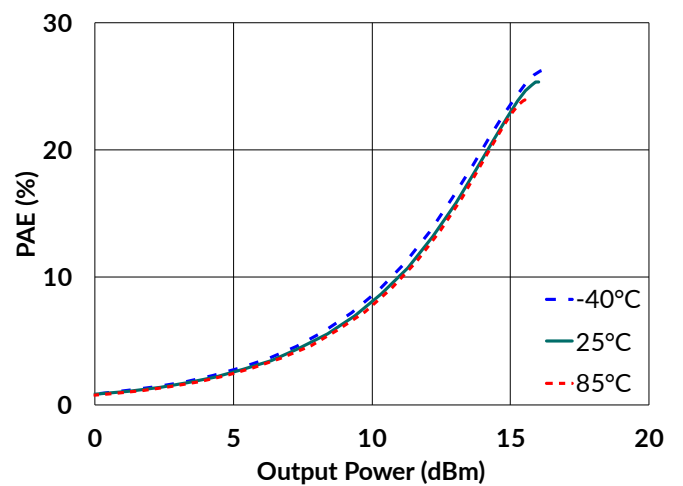
PAE vs Output Power at 16 GHz



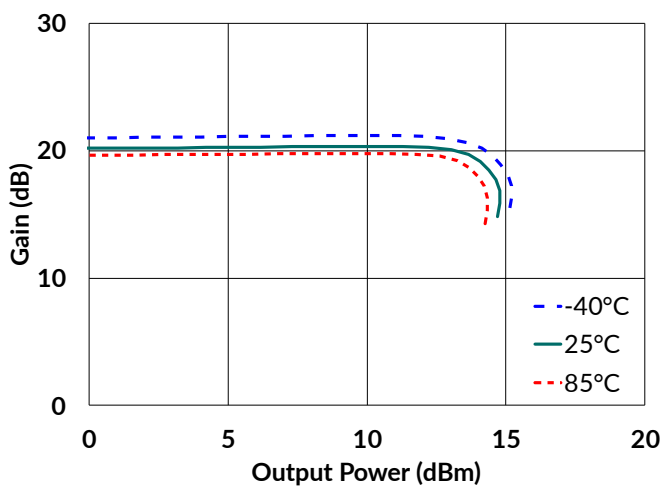
Gain vs Output Power at 22 GHz



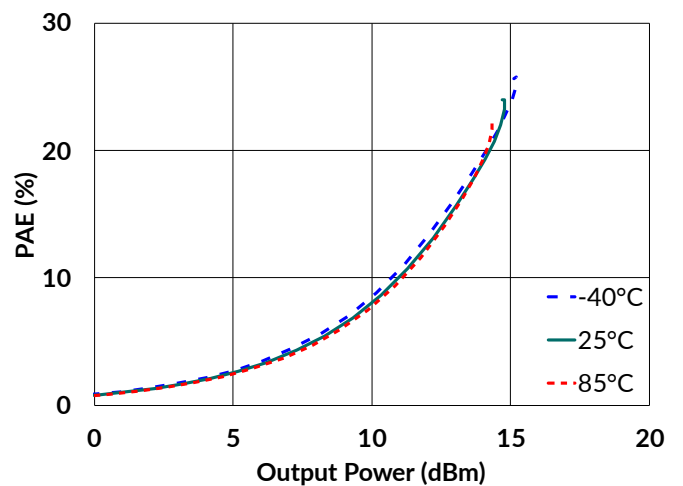
PAE vs Output Power at 22 GHz



Gain vs Output Power at 25 GHz



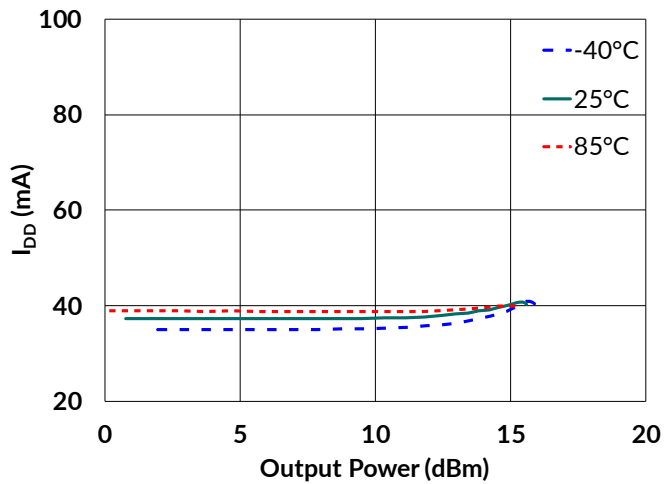
PAE vs Output Power at 25 GHz



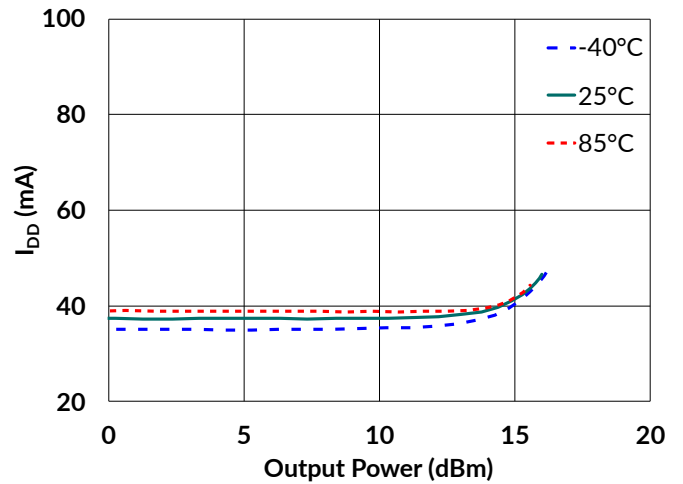
Measured Performance – Large Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 3.3\text{ V}$ ($I_{DDQ} \approx 65\text{ mA}$)

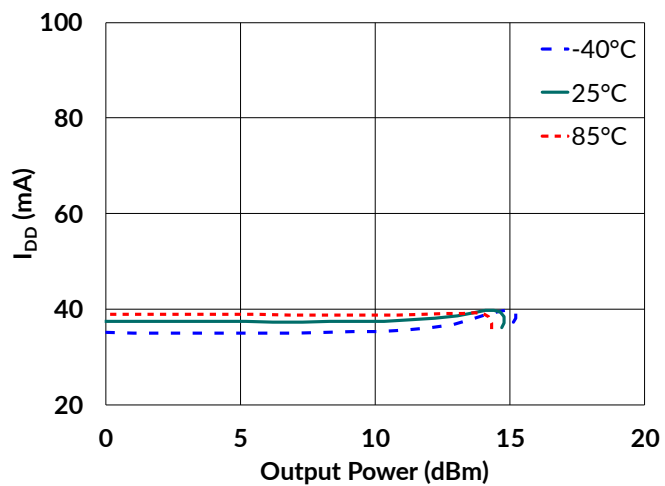
I_{DD} vs Output Power at 16 GHz



I_{DD} vs Output Power at 22 GHz



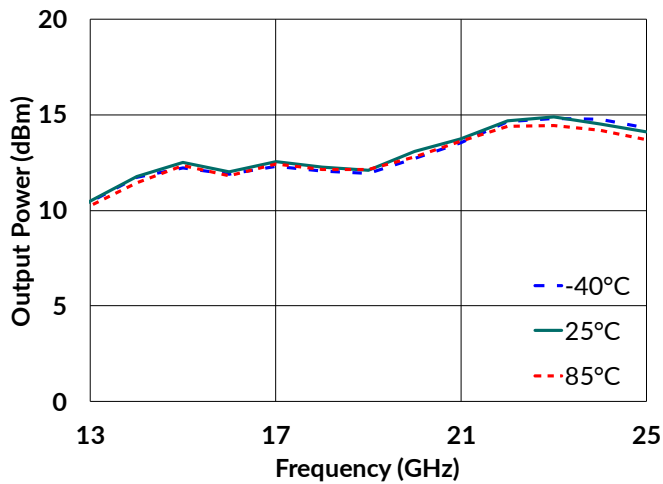
I_{DD} vs Output Power at 25 GHz



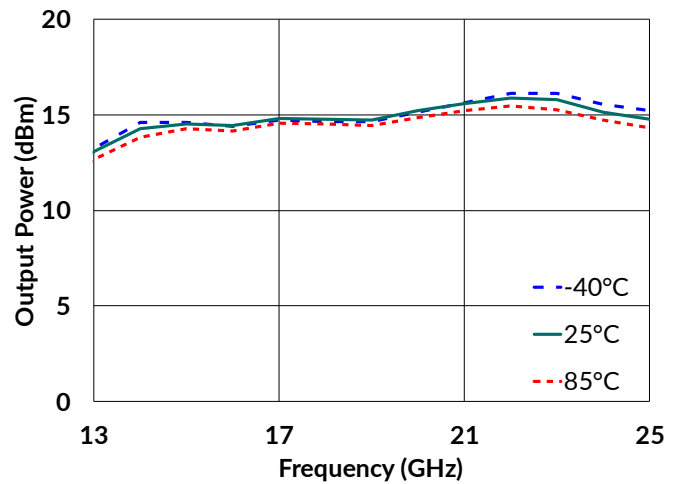
Measured Performance – Large Signal

Nominal Bias: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 3.3\text{ V}$ ($I_{DDQ} \approx 65\text{ mA}$)

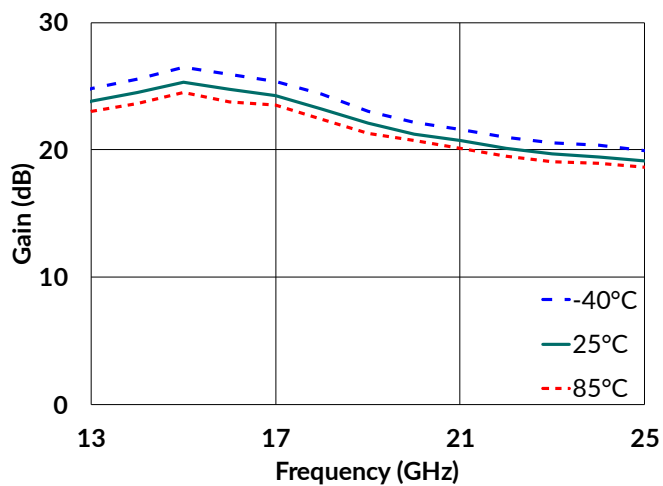
Output P1dB



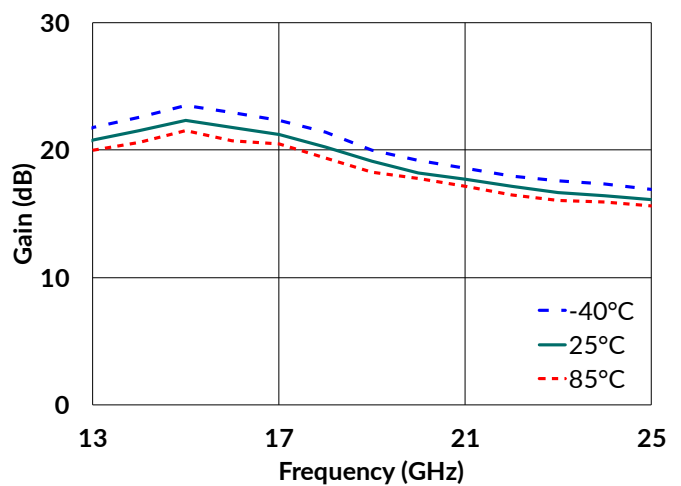
Output P3dB



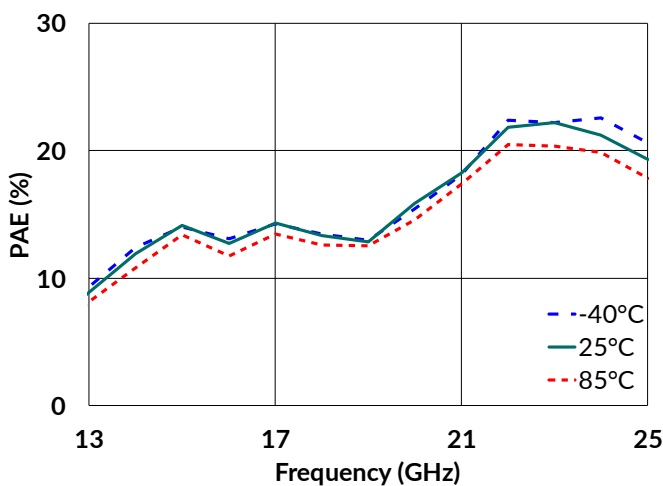
Gain P1dB



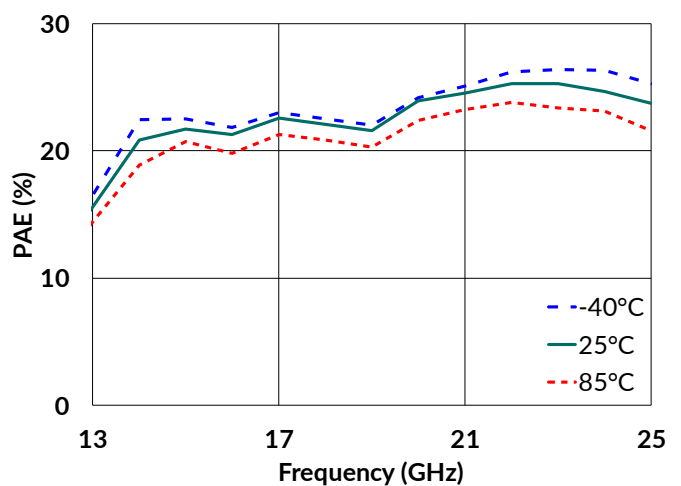
Gain P3dB



PAE P1dB



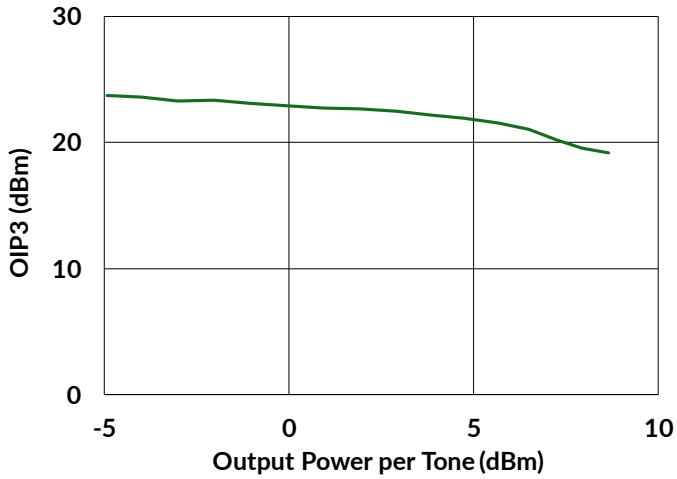
PAE P3dB



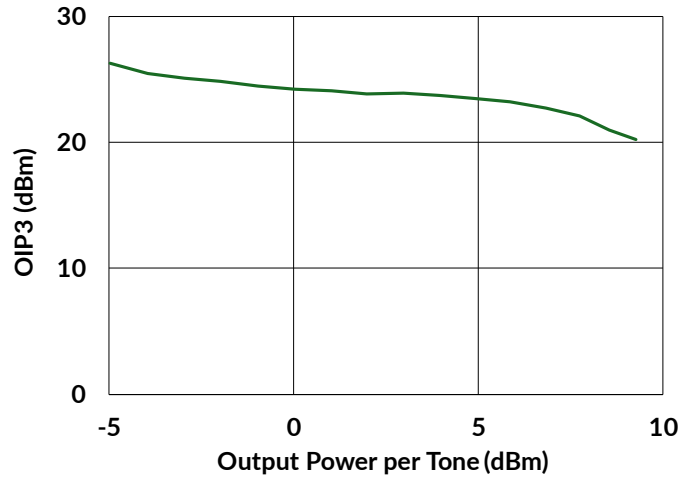
Measured Performance – Linearity

Room Temperature: $V_{DD} = 3.3\text{ V}$, $V_{BIAS} = 2.5\text{ V}$ ($I_{DDQ} \approx 40\text{ mA}$), $\Delta F = 10\text{ MHz}$

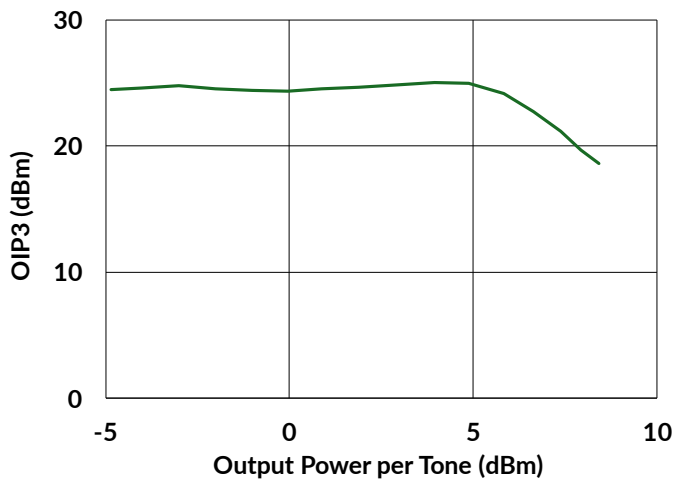
OIP3 versus P_{OUT}/tone at 16 GHz



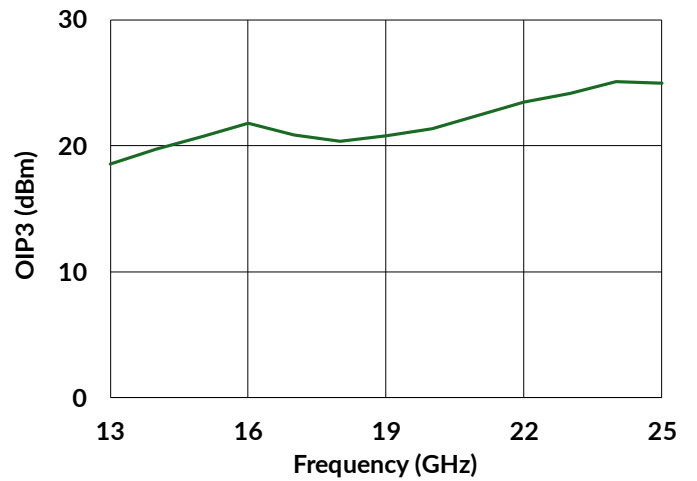
OIP3 versus P_{OUT}/tone at 22 GHz



OIP3 versus P_{OUT}/tone at 25 GHz



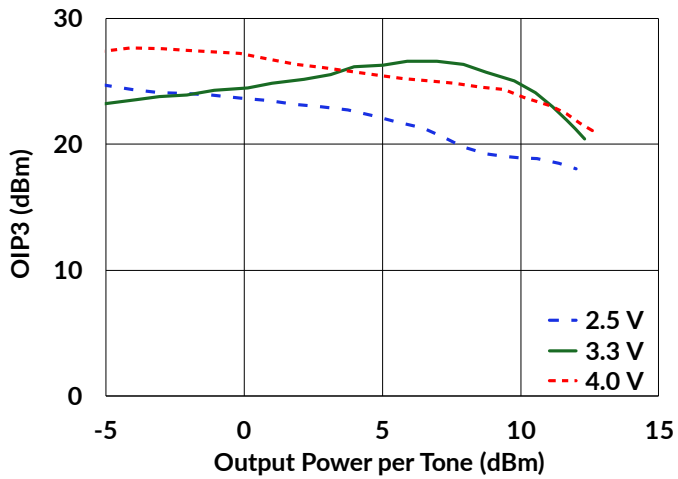
OIP3 at $P_{OUT}/\text{tone} = +5\text{ dBm}$



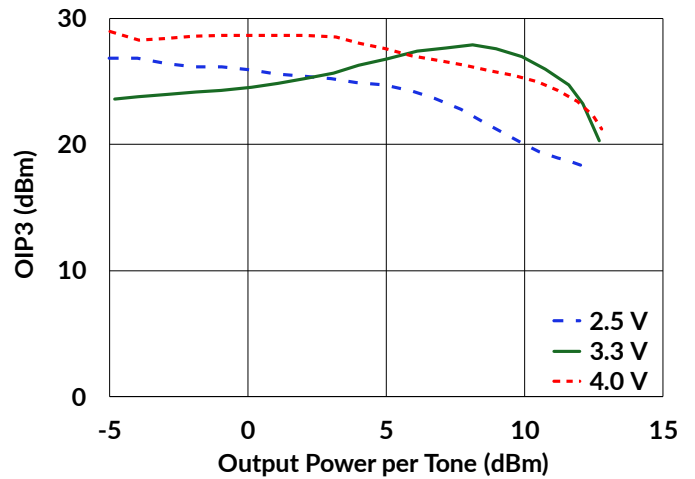
Measured Performance – Linearity

Room Temperature: $V_{DD} = 4\text{ V}$, $V_{BIAS} = 2.5, 3.3\text{ and }4\text{ V}$ ($I_{DDQ} \approx 40, 65\text{ and }85\text{ mA}$), $\Delta F = 10\text{ MHz}$

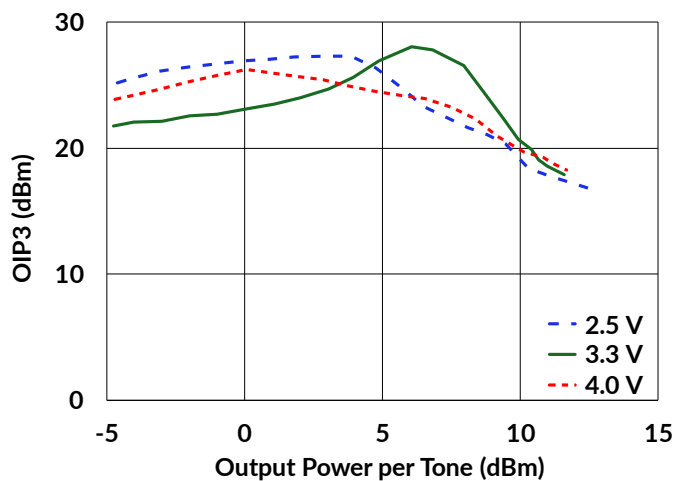
OIP3 versus P_{OUT}/tone at 16 GHz



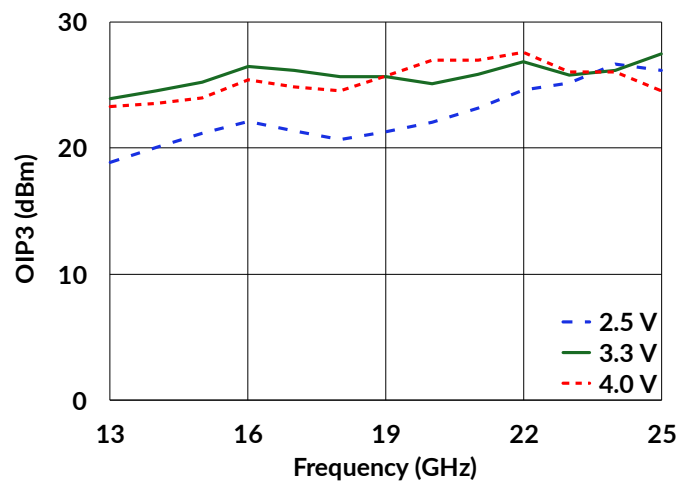
OIP3 versus P_{OUT}/tone at 22 GHz



OIP3 versus P_{OUT}/tone at 25 GHz



OIP3 at $P_{OUT}/\text{tone} = +5\text{ dBm}$



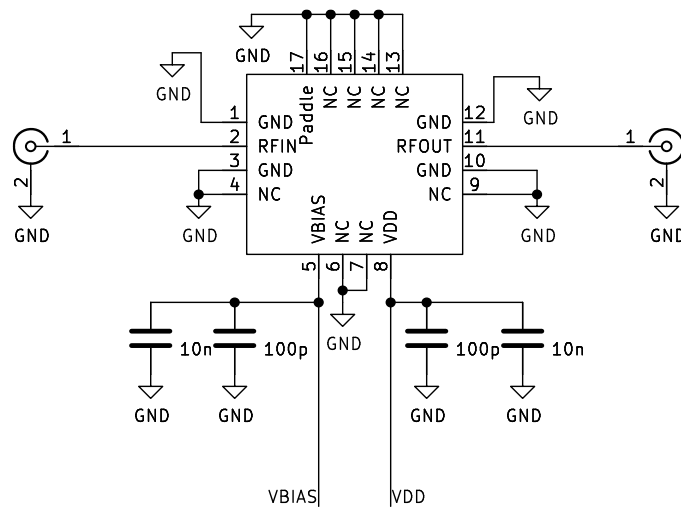
Application Schematic

Biasing

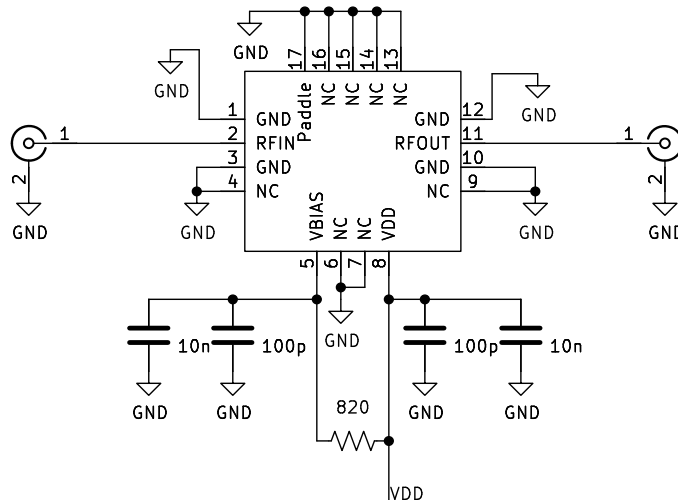
ARF1205Q2 has two biasing methods. The first is V_{DD} and V_{BIAS} which can be biased with separate power supplies. By altering V_{BIAS} the current of V_{DD} will change the performance. The second method ties V_{BIAS} to V_{DD} via a resistor. The value of the resistor determines the current of the device and some resistor and current values are provided in the evaluation board section. This method enables the ARF1205Q2 to be biased by a single supply.

Additionally, while the exact bypass network will be customer specific, we recommend as a minimum to have a 100 pF capacitor and 10 nF capacitor on both the V_{DD} and V_{BIAS} lines.

The Altum RF evaluation board ships with pads for biasing via a resistor but typically this isn't populated.

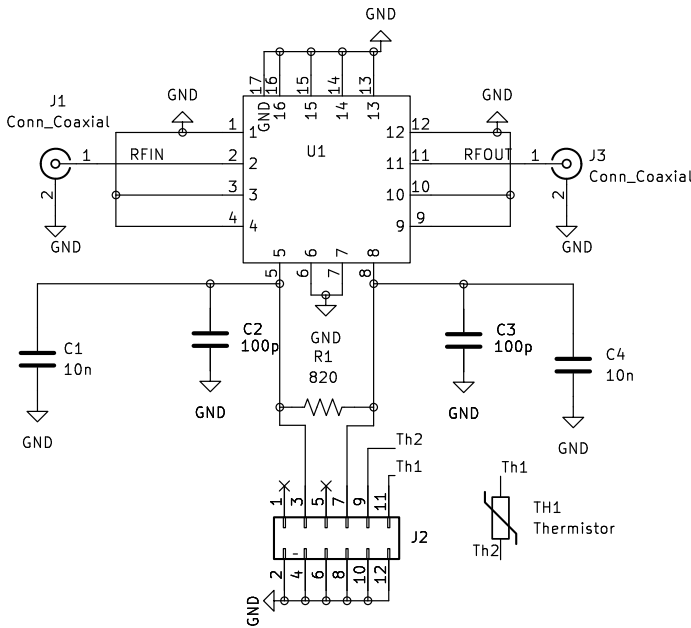


Individual Biasing of V_{DD} and V_{BIAS}



Biasing through resistor

Evaluation Board Schematic



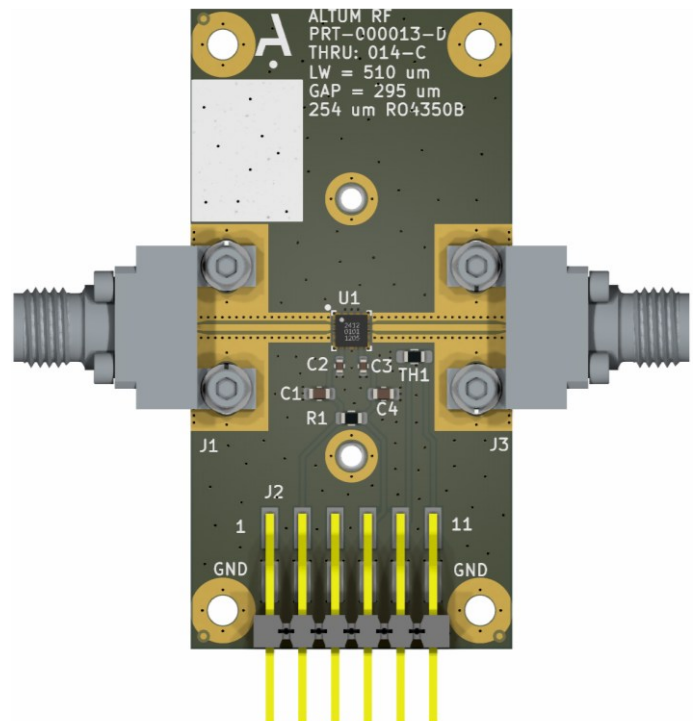
J2 Pin	Description
3	V_{BIAS}
7	V_{DD}
1,5	Unconnected
9,11	Thermistor (optional)
2,4,6,8,10,12	Ground

Bias Control ⁶			
V_{DD} (V)	I_{DD} (mA)	V_{BIAS} (V)	R1 (Ω)
3.3	65	3.3	0
3.3	40	2.5	820
4.0	85	4.0	0
4.0	65	3.3	560
4.0	40	2.5	1.8k

Bill of Materials

Description	Reference Designator	Quantity
ARF1205Q2	U1	1
10 nF 0603 Capacitor	C1,C4	2
100 pF 0402 Capacitor	C2,C3	2
820 Ω 0603 Resistor (optional)	R1	1
12 pin Samtec TSM-106-01-F-DH-P	J2	1
Southwest Microwave 2.92mm 1092-01A-6 or equivalent	J1,J3	2

Evaluation Board Layout



Recommended land-pattern and sample board layout for 254 μm thick RO4350 are available on request. Contact Altum RF Application Support for further information.

6. V_{BIAS} can be supplied externally or can be generated using the resistor R1 between the V_{DD} rail and the V_{BIAS} pin.

Application Notes

1. Bias Turn-on Sequence

V_{DD} and V_{BIAS} can be safely applied in any order, or simultaneously.

The part has internal bias regulation. V_{BIAS} can be supplied externally or can be generated using the resistor R1. Refer to Bias Control table for suggested operating bias condition.

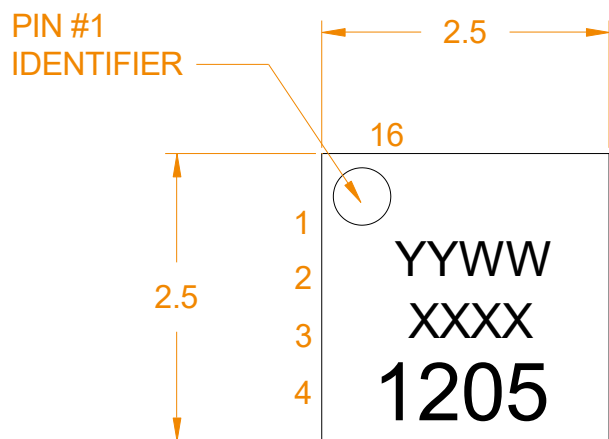
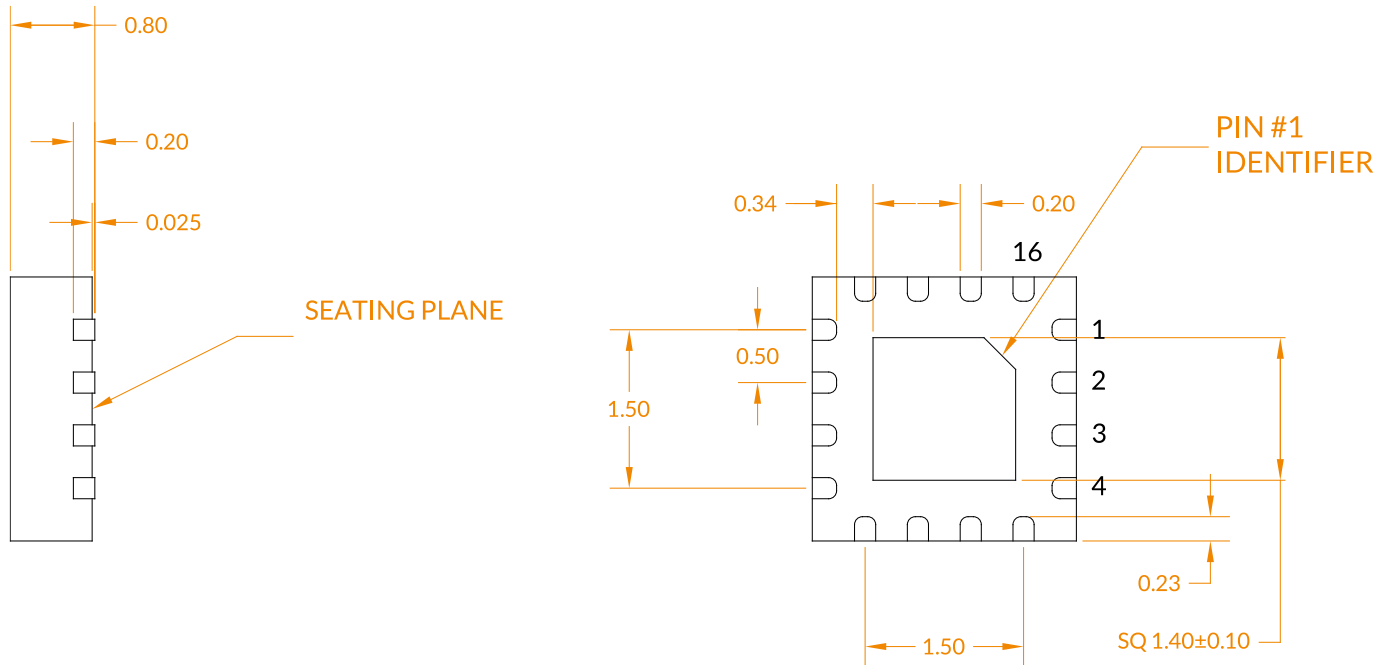
The part can be turned off by applying 0 V to V_{BIAS} or to V_{DD} .

2. Reflow Information

MSL level 1 as per IPC/JEDEC J-STD-020E.

Package Information

Outline Drawing



YYWW is the date code

XXXX is the lot code

1205 is the part number

All dimensions are in millimeters.
Package leads and exposed pad are plated with NiPdAu.

Ordering Information

Part Number	Delivery Format	Quantity
ARF1205Q2-TR500	Tape and Reel	500 pcs
ARF1205Q2-TR2500	Tape and Reel	2500 pcs

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Preliminary: Measured performance based on prototype parts. Specifications including maximum and minimum values are subject to change.
Final: Guaranteed performance of qualified and production released part.